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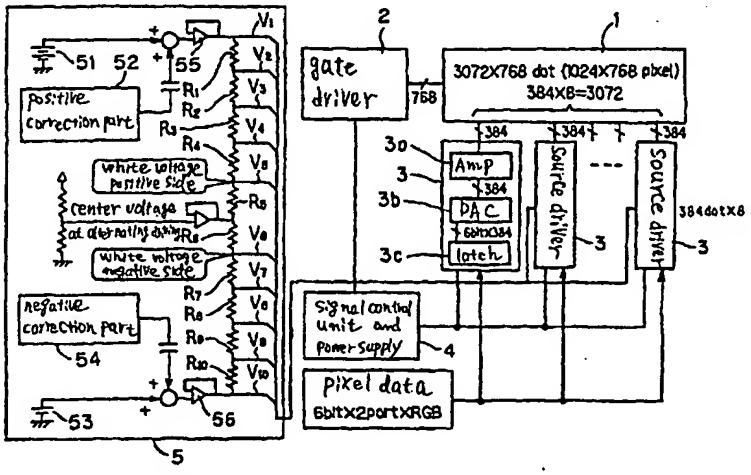

(57) Abstract: The invention concerns an active matrix LCD with subpixels, where a polarity inversion scheme is applied, such as every two rows and one column. Column drivers receive as input digital image signals and comprise a D/A converter that selects among voltages generated by a reference potential generation circuit having positive and negative power supplies and resistor ladder. A problem exists in that parasitic capacitances between neighbouring subpixels have a coupling effect that causes alterations of the applied voltages, which results in e.g. appearance of stripes in image portions that should appear uniform instead. In the present invention, such problem is solved by the addition of suitable positive and negative correction voltages to the positive and negative power supply voltages of the reference potential generation circuit. Such correction voltages are selected such to compensate the alterations to pixel voltages caused by said parasitic capacitances.

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LIQUID CRYSTAL DISPLAY DEVICE WITH DRIVING VOLTAGE CORRECTION FOR REDUCING NEGATIVE EFFECTS CAUSED BY CAPACITIVE COUPLING BETWEEN ADJACENT PIXEL ELECTRODES

The invention relates to a liquid crystal display device comprising a first substrate provided with plural pixel electrodes and a second substrate provided with a common electrode.

In a liquid crystal display device, a voltage is applied on a liquid crystal to drive the liquid crystal. For preventing the degradation of liquid crystal, an alternating voltage is applied to the liquid crystal. Conventionally, a frame-alternating drive has been known as one of the methods for driving a liquid crystal. In this frame-alternating drive, however, there is a problem that flicker is easily occurred. For taking countermeasures against the flicker, alternatively, other methods have been used for driving a liquid crystal by applying a voltage on the liquid crystal so that the polarities of the neighboring pixels becomes opposite with respect to each other, including a line-alternating drive method, a row-alternating method, and a pixel-alternating drive method.

However, depending on the pattern of the image or the color of the image to be displayed, there may be cases where troubles such as crosstalk and flicker are caused even if the drive method where the polarities of the neighboring pixels becomes opposite with respect to each other, such as a line-alternating drive method, a row-alternating method, and a pixel-alternating drive method, is used. To solve the problems, there is an idea of driving the liquid crystal by using for example the 2 column-1 row alternately driving method (hereinafter referred to as "2 column-1 row method" for short).

Fig.8 shows a conceptual rendering of 2 column-1 row method.

In each frame, as shown in Fig. 8, the polarities of the respective pixels placed in a row direction are defined so that two adjacent pixels have the same polarity and the polarities of the pixels are varied every two pixels. The polarity of each pixel in the odd-numbered frame is opposite to the corresponding pixel of the even-numbered frame.

The 2 column-1 row method causes less troubles such as crosstalk and flicker in comparison with the other methods such as line-, row-, and pixel-alternating drive. However, in the 2 column-1 row method, there is another problem to be caused. If a liquid crystal display shows an image filled with a substantially constant lightness of color, such as an image of blue sky, the display would be expected to show an image having evenly

distributed lightness of color. Nevertheless, in some cases, there is a problem that a phenomenon where light column and dark column occur alternately (hereinafter referred to as horizontal stripes) is recognized.

The object of the present invention is to provide a liquid crystal display device that hardly displays horizontal stripes, even though the liquid crystal display device displays an image filled with a substantially constant lightness.

A liquid crystal display device according to the present invention, which is comprising a first substrate provided with plural pixel electrodes to which a potential is applied via a same data line, a second substrate provided with a common electrode, said second substrate for sandwiching liquid crystal between the first substrate and the second substrate, and potential application means for applying the potential to the plural pixel electrodes on the basis of plural pixel data,

wherein the potential application means corrects the potential to be applied to the plural pixel electrodes on the basis of coupling capacitance formed between mutually adjacent pixel electrodes.

In the present invention, furthermore, the term "pixel electrode" denotes not only a pixel electrode which is formed so as to be correspond to each dot in a black-and-white image where one pixel is constructed of one dot but also a sub-pixel electrode which is formed so as to be correspond to each dot in a color image where one pixel is constructed of two or more dots, for example one pixel is constructed of three dots. Further, in the present invention, the term "pixel data" denotes not only a pixel data which is correspond to each dot in the case that one pixel is constructed of one dot but also a sub-pixel data which is correspond to each dot in the case that one pixel is constructed of two or more dots.

As will be described later, a coupling capacitance formed between pixel electrodes adjacent to each other may become a cause of horizontal stripes. Therefore, an image can be shown without causing horizontal stripes thereon if a voltage is applied on each pixel electrode on the basis of a coupling capacitance, as described above.

Preferably, in the liquid crystal display device according to the present invention, wherein the potential application means has reference potential generation means for generating reference potentials and reference potential correction means for correcting the reference potentials generated by the reference potential generation means on the basis of the coupling capacitance, the potential application means generates a plural potentials from the corrected reference potentials, selects each of potentials corresponding to each of the plural

pixel data from the plural potentials, and applies these selected potentials to the plural pixel electrodes.

The generation of horizontal stripes may be avoided by correcting a potential to be generated from the reference potential generation means on the basis of the coupling capacitance.

Preferably, in the liquid crystal display device according to the present invention, wherein the reference potential generation means generates plural reference potentials by ladder resistance.

A plural reference potentials can be easily obtained by the use of a ladder resistance.

Preferably, in the liquid crystal display device according to the present invention, wherein the reference potential correction means corrects the potential generated by the reference potential generation means at an intermediate position of the ladder resistance.

Considering the voltage-light transmission characteristics of the liquid crystal, the extent of variations in the light transmission with respect to the extent of variations in voltage is large at a region corresponding to a halftone. However, the extent is small at a region close to the side of white or black. Therefore, even if a signal to be generated from the reference potential generation means is corrected at an intermediate position of the ladder resistance, the voltage of a pixel electrode can be corrected with a high degree of precision as long as the intermediate position is near the end of the ladder resistance.

Further, in the liquid crystal display device according to the present invention, wherein the potential application means has reference potential generation means for generating reference potentials and data correction means for correcting the plural pixel data on the basis of the coupling capacitance, the potential application means generates a plural potentials from the corrected reference potentials, selects each of potentials corresponding to each of the corrected plural pixel data from the plural potentials, and applies these selected potentials to the plural pixel electrodes.

The potential to be applied on the pixel electrode can be corrected by correcting pixel data itself instead of the potential to be generated from the reference potential generation means.

Hereinafter, we will describe the mode for carrying out the invention.

Fig. 1 is a block diagram that illustrates the configuration of a liquid crystal display device as one mode for carrying out the invention.

The liquid crystal display device has a liquid crystal panel 1. The liquid crystal panel 1 comprises a thin-film transistor (TFT) substrate (not shown) provided with pixel electrodes and a color filter substrate (not shown) provided with common electrode. Liquid crystal is sandwiched between these substrates. The liquid crystal panel 1 has (3072 x 768) sub-pixels, each of sub pixel electrodes is constructed of three sub-pixels R(Red), G(Green)and B(Blue). That is to say, The liquid crystal panel 1 has 1027 x 768 =786,432 pixels which arranged in the matrix form.

Fig. 2 is an enlarged view of a part of the TFT substrate of the liquid crystal panel 1 shown in Fig. 1.

In this figure, a portion of the TFT substrate which correspond to the sub-pixels R(red) of the pixels n, n + 1, and n + 2 is shown. In addition, a gate bass extends between the sub-pixels adjacent to each other. In this figure, four gate buses Gn – 1, Gn, Gn + 1, and Gn + 2 are shown. Further, source bus S (which corresponds to data line in the present invention) extends across those gate buses in a vertical direction. Furthermore, sub-pixel electrodes (which correspond to pixel electrodes in the present invention) En, En + 1, and En + 2 are formed in the area which correspond to the sub-pixels R of the pixels n, n + 1, and n + 2, respectively. And TFT (Thin Film Transistor) (n), TFT (n + 1), and TFT (n + 2) are formed in the area which correspond to the sub-pixels R of the pixels n, n + 1, and n + 2, respectively. The TFT(n), TFT (n + 1), and TFT (n + 2) control the transition of signals passed through the source bus S to each of the sub-pixel electrodes En, En + 1, and En + 2. If each of TFT (n), TFT (n + 1), and TFT (n + 2) enters the ON state, the signals passed through the source bus S are transmitted to the sub-pixel electrodes En, En + 1, and En + 2, respectively. If each of TFT (n), TFT (n + 1), and TFT (n + 2) enters the OFF state, the signals passed through the source bus S are not transmitted to the sub-pixel electrodes En, En + 1, and En + 2, respectively.

Fig. 2 shows the structure of the portion corresponding to the sub-pixels R. In this embodiment, it is noted that the sub-pixels G and the sub-pixels B also have the same structure as that of the portion corresponding to the sub-pixels R.

Referring back to Fig. 1, the liquid crystal display device of the present embodiment will be further described in detail.

A gate driver 2 and eight source drivers 3 are positioned around the liquid crystal panel 1. Each source driver 3 comprises an amplifier 3a, a digital-to-analog converter (DAC) 3b, and a latch 3c. In the liquid crystal display device, furthermore, a signal control unit and an power supply (hereinafter referred to as signal power supply) 4 are provided. The

signal power supply 4 supplies power supply voltage to the gate driver 2 and the source driver 3, and also supplies control signals to the gate driver 2 and the source driver 3. Each of the source drivers 3 receives 6 bit sub-image data.

The liquid crystal display device further comprises a gamma-correction reference potential generation circuit (hereinafter, referred to simply as a potential generation circuit) 5 for supplying a reference potential to each of the source drivers 3. The potential generation circuit 5 comprises a positive-side electric power supply 51 and a negative-side electric power supply 53. These electric power supplies 51 and 53 are connected to ladder resistances R1-R10 connected in series through amplifiers 55 and 56, respectively. In addition, the potential generation circuit 5 comprises a signal generation part for correcting positive-side (hereinafter, referred to simply as a positive correction part) 52 and a signal generation part for correcting negative-side (hereinafter, referred to simply as a negative correction part) 54. These positive and negative correction parts 54, 55 correspond to reference potential correction means of the present invention. The positive correction part 52 generates a rectangular signal for correcting a potential supplied from the positive-side electric power supply 51 on the basis of a coupling capacitance (described later) formed between the sub-pixels adjacent to each other. On the other hand, the negative correction part 54 generates a rectangular signal for correcting a potential supplied from the negative-side electric power supply 53 on the basis of a coupling capacitance described later.

The potential supplied from the positive-side electrode 51 is corrected with the addition of the rectangular signal generated from the positive correction part 52. The corrected potential becomes a reference potential V1 through the amplifier 55. On the other hand, the potential supplied from the negative-side electric power supply 53 is corrected with the addition of the rectangular signal generated from the negative correction part 54. The corrected potential becomes a reference potential V10 through the amplifier 56. Furthermore, the potentials passing through their respective amplifiers 55, 56 are resistance-divided by the ladder resistances R1 to R10, resulting in the generation of reference potentials V2 to V9, respectively. Consequently, ten reference potentials V1 to V10 are generated. Among the reference potentials V1 to V10, the reference potentials V1 to V5 are larger than the alternating central potential. On the other hand, the reference potentials V6 to V10 are smaller than the alternating central potential. Hereinafter, the reference potentials V1 to V5 may be referred to as positive reference potentials, while the reference potentials V6 to V10 may be referred to as negative reference potentials. Each of generated reference potentials V1 to V10 is introduced into the DAC 3b of each source bus 3. The DAC 3b

generates many potentials by resistance-dividing the potential generated from the potential generation circuit 5, and selects a potential to be supplied to each sub-pixel electrode from the above-mentioned many potentials.

The operation of the liquid crystal display device shown in Fig. 1 will be described as follows.

Control signals are supplied from the control electric power supply 4 to the gate driver 2 and the source drivers 8, respectively. The gate driver 2 transfers signals for turning on the TFT to each of the gate buses (see Fig. 2) on the basis of the control signals. When each of the source drivers 3 receives its control signal, a latch 3c of each source driver 3 latches 6-bit sub-pixel data. Then the sub-pixel data being latched in the latch 3c is successively sent to the DAC 3b. In addition, the control power supply 4 generates a polarity control signal for controlling whether DAC3b selects the potential from many potentials generated by resistance-dividing the positive reference potentials V1-V5 or selects the potential from many potentials generated by resistance-dividing the negative reference potentials V6-V10. The polarity control signal is supplied to the DAC 3b. The DAC 3b selects a potential corresponding to the sub-pixel data from many potentials obtained by resistance-dividing the potential generated from the potential generation circuit 5, on the basis of the polarity control signal and the sub-pixel data. If the potential is selected by the DAC 3b, the current corresponding to the selected potential is amplified by the amplifier 3a and then transferred to the corresponding source bus S (see Fig. 2). When the TFT turns on by the signal transferred to the gate bus, the signal representing the potential transferred to the source bas S is transferred to each sub-pixel electrode through the TFT. By this, the potential corresponding to each of the sub-pixel data is applied to each of the sub pixel electrodes. Consequently, a voltage is applied to liquid crystal layer sandwiched between the common electrode and each sub-pixel electrode. The liquid crystal layer can be driven in response to the potential supplied on each sub-pixel electrode, the image is displayed on the liquid crystal panel 1.

Here, we will consider a conventional liquid crystal display device. The difference between the conventional liquid crystal display device and the liquid crystal display device showing in Fig. 1 is only as follows; the conventional liquid crystal display does not comprise the positive correction part 52 and the negative correction part 54. When an image having even brightness, such as a blue sky is displayed on a screen of the conventional liquid crystal display, light and dark patterns alternately occur in the extending

direction of the source bus over the screen. We will describe the cause of occurrence of the light and dark patterns with reference to Figs. 2 to 6.

In the case that an image having even lightness, such as an image of blue sky, is displayed on the panel, all sub-pixels which display the same colour (that is, red or green or blue) must show the same lightness. Thereinafter, in the case of displaying the red having equal lightness on all sub-pixels for displaying R (red), the state of applying potentials on the respective sub-pixel electrodes En, En + 1, and En + 2 (see Fig. 2) will be described with reference to Fig. 3 in addition to Fig. 2.

Fig. 3 is a timing chart showing the timing when the potentials are applied to the respective sub-pixel electrodes En, En + 1, and En + 2.

Each of the gate buses Gn-1, Gn, Gn+1, and Gn + 2 receives a signal containing pulses P1, P2 (having a potential Vg) which alternately occurring every one vertical period. Each of the pulses P1, P2 generated at each of the gate buses generates at the timing delayed only one horizontal period, compared with the preceding gate bus. During the period which the pulses P1, P2 occur in each of the gate buses Gn-1, Gn, Gn+1, and Gn+2, the corresponding TFT enters its ON state.

The source bus S receives a signal in which rectangular waves of periodicity T occur repeatedly. The rectangular wave of periodicity T is represented by both a potential Vsp which is larger than a potential Vcom (= constant) of the common electrode and a potential Vsn which is smaller than the potential Vcom of the common electrode. That is, the source bus S receives a signal in which pulse having a potential (Vsp – Vsn) occurs repeatedly.

By the way, the source bus, the gate bus, the electrode, and the like are formed in each of portion corresponding to each sub-pixel. These bus and electrode form capacitance such as parasitic capacitance Cgd caused by the gate and drain electrodes of the TFT, storage capacitance Cs, a sub-pixel capacitance Clc caused by the sub-pixel electrode and the common electrode, and coupling capacitance Cdd formed by the sub-electrodes adjacent to each other. In Fig. 2, the capacitance Cgd, Cs, Clc, and Cdd formed on the portions of the pixel corresponding to the sub-pixels are shown with the subscripts n, n + 1, and n + 2, respectively. In addition, the total capacitance Ct (i) (i = 1, 2, 3, ... n-1, n, n + 1, n + 2, ...) of one sub-pixel R (i) (hereinafter, the total capacitance is referred to as the sub-pixel capacitance) is represented by the following equation.

$$Ct(i) = Cgd(i) + Cs(i) + Clc(i) + Cdd(i) + Cdd(i+1) \quad .....(1)$$

In this equation (1), Cgd(i) takes the same value for each of the sub-pixels when the sub-pixels are equal to each other with respect to the lightness. Therefore, in the following description, Cgd(i) is constant regardless of the value of "i". Thus, Cgd(i) may be simply denoted by Cgd, except for the case that there must be a need to clarify which sub-pixels does Cgd exist in. Further, each of Cs(i), Clc(i), and Cdd(i) takes the same value for each of the sub-pixels when the sub-pixels are equal to each other with respect to the lightness. Therefore, regarding Cs (i), Clc (i), and Cdd (i), they may be simply denoted by Cs, Clc, and Cdd, respectively, except for the case that there must be a need to clarify which sub-pixels dose each of Cs, Clc, and Cdd exist in.

Among four types of capacitance, Cgd, Cs, Clc, and Cd, we assume that the coupling capacitance Cdd is absence while other three types of the capacitance Cgd, Cs, and Clc are presence (therefore, Ct is represented by Cgd + Cs + Clc). In such a situation, we consider a example that signal shown in Fig. 3 are transmitted to the source bus and the gate bus. In this case, a potential waveform of the sub-pixel electrode En (see Fig. 2) can be represented as a potential waveform (1). That is, in the sub-pixel electrode En, a potential with the amplitude of "A", which is correspond to the pulse P1 (potential Vg) of the gate bus Gn - 1, is firstly generated through the storage capacitance Cs (n) (where A = Vg x Cs (n) / Ct (n)). Then, the pulse P1 of the gate bus Gn is generated during the period of t1 to t2, and then the TFT (n) (see Fig. 2) becomes ON state during only the time corresponding to a pulse width of the pulse P1. Consequently, a potential Vsp (hereinafter, this potential may be referred to as a positive potential) is supplied to the sub-pixel electrode En from the source bus S via TFT (n). Therefore, During the period K1 of generating the pulse P1 of the gate bus Gn (during the period K1, the TFT (n) is in the ON state), the potential Vsp is temporarily written in the sub-pixel electrode En (at the time t2). However, the potential Vn (n) of sub-pixel electrode En reduces by the kickbag amount ΔVc (= Vg x Cgd (n) / Ct (n)) because of the influence of storage capacitance Cgd (n) (at the time t2). As a result, the potential of the sub-pixel electrode En is eventually kept the value represented by the following equation (2).

$$V(+) = Vsp - \Delta Vc \quad \ldots\ldots (2)$$

In the following description, the potential eventually kept in the sub-pixel electrode when the positive potential is applied on the sub-pixel electrode is referred to as a positive writing potential. Subsequently, a potential with the amplitude of "A", which is correspond to the pulse P2 occurring after one vertical period from the Pulse P1 of the gate bus Gn–1, is generated through the accumulated capacitance Cs (n). Then, the pulse P2 of the gate bus Gn

is generated during the period of t5 to t6, and then the TFT (n) becomes the ON state during the only time corresponding to a pulse width of the pulse P2. Consequently, a potential Vsn (hereinafter, the potential Vsn may be referred to as a negative potential) is supplied to the sub-pixel electrode En from the souse bus S via the TFT (n). During the period K2 where the pulse P2 of the gate bus Gn is generating (i.e. the period where the TFT (n) is in the ON state), therefore, the potential Vsn instead of the potential V (+) is temporarily written in the sub-pixel electrode En (at the time t6). However, the potential Vn (n) of sub-pixel electrode En reduces by the kickbag amount ΔVc (at the time t6) because of the influence of storage capacitance Cgd (n) (at the time t6). As a result, the potential of the sub-pixel electrode En is eventually kept the value represented by the following equation (3).

$$V(-) = Vsn - \Delta Vc \quad \ldots. (3)$$

In the following description, the potential eventually kept in the sub-pixel electrode when the negative potential is applied on the sub-pixel electrode is referred to as a negative writing potential.

Through the actions described above, the positive-writing potential V (+) and the negative-writing potential V(-) are alternately occurred in the sub-pixel electrode En every time one pulse is generated at the gate bus Gn. As a result, potential waveform (1) is repeatedly appeared at the sub-pixel electrode En. The potential of the common electrode is Vcom, so that a positive voltage $Vsp - \Delta Vc - Vcom$ is applied on the liquid crystal of the sub-pixel R (n) when the potential of the sub-pixel electrode En is a positive-writing potential $V(+) = Vsp - \Delta Vc$, while a negative voltage of $Vcom - Vsn + \Delta Vc$ is applied on the liquid crystal of the sub-pixel R (n) when the potential of the sub-pixel electrode En is a negative-writing potential $V(-) = Vsn - \Delta Vc$. By the way, in order to apply the voltage having same absolute value to the sub-pixel R(n) regardless of the polarity of voltage to be applied to the liquid crystal of the sub-pixel (R), Vcom is set to the value that satisfies the equation of the positive voltage (Vsp – ΔVc – Vcom) = the negative voltage (Vcom – Vsn + Vc). That is to say, the following equation (4) is satisfied.

$$Vcom = (Vsp + Vsn) / 2 - \Delta Vc \quad \ldots..(4)$$

As can be seen from the above description, the potential difference between the positive writing potential $V(+) = Vsp - \Delta Vc$ and the negative writing potential $V(-) = Vsn - \Delta Vc$ can be represented by the following equation (5).

$$Va = Vsp - Vsn \quad \ldots.(5)$$

In the following description, the potential difference between the positive writing potential and the negative writing potential of each sub-pixel potential is referred to as a writing potential difference.

Now, we will consider a potential waveform of the sub-pixel electrode En+1.

Pulses P1, P2 are appeared in the gate bus Gn + 1 after a delay of one horizontal period from those of the gate bus Gn. At this time, the potential of the source bus S is a positive potential Vsp during the period K3 where the pulse P1 is generated in the gate bus Gn+1, and the potential of the source bus S is a negative potential Vsn during the period K4 where the pulse P2 is generated in the gate bus Gn+1. During the period K3, therefore, the positive potential Vsp is written in the sub-pixel electrode En+1 with a timing corresponding to a delay of one horizontal period with respect to the preceding electrode En (at the time t3). During the period K4, on the other hand, the negative potential Vsn is written in the sub-pixel electrode En+1 with a timing corresponding to a delay of one horizontal period with respect to the preceding electrode En (at the time t7). Consequently, the potential waveform (2) of the sub-pixel electrode En+1 has the same form as the potential waveform (1) of the sub-pixel electrode En, in addition to, the potential waveform (2) is shifted by just one horizontal period with respect to the potential waveform (1) in the direction of causing a time delay.

Then, we will consider a potential waveform of the sub-pixel electrode En+2.

Pulses P1, P2 are appeared in the gate bus Gn+2 after a delay of one horizontal period from those of the gate bus Gn+1. At this time, the potential of the source bus S is a negative potential Vsn during the period K5 where the pulse P1 is generated in the gate bus Gn+2, and the potential of the source bus S is a positive potential Vsp during the period K6 where the pulse P2 is generated in the gate bus Gn+2. During the period K5, therefore, the negative potential Vsn, which is opposite to that of the preceding sub-pixel electrode En+1, is written in the sub-pixel electrode En+2 (at the time 4). During the period K6, on the other hand, the positive potential Vsp, which is opposite to that of the preceding sub-pixel electrode En+1, is written in the sub-pixel electrode En+2 (at the time t8). Consequently, in the potential waveform (3) of the sub-pixel electrode En+2, its positive and negative writing potentials appear contrarily in comparison with the potential waveforms (1), (2) of their respective sub-pixel electrodes En, En+1.

There are no concrete illustrations concerned about potential waveforms of the sub-pixel electrode En+3 which is subsequent to the sub-pixel electrode En+2. However, the potential waveforms of the sub-pixel electrode En+3 can be considered just as in the case of

the potential waveform (3) of the sub-pixel electrode En+2. That is, the potential waveform of the sub-pixel electrode En+3 has the same form as the potential waveform (3), in addition to, the potential waveform of the sub-pixel electrode En+3 is shifted by just one horizontal period with respect to the potential waveform (3) in the direction of causing a time delay.

Regarding the sub-pixel electrodes En+4, En+5 and so on which are subsequent to the sub-pixel electrode En+3, the potential waveforms of the sub-pixel electrode En+4, En+5 and so on are represented by the waveforms which are the same form as the potential waveform of the sub-pixel electrode En, En+1, En+2 are shifted by just one horizontal period in the direction of causing a time delay. Therefore, as to each of the sub-pixel electrodes, their difference potentials between the positive writing electrode and the negative writing electrode have the same potential difference Va = Vsp – Vsn (see the equation (5)).

As described above, we can drive the liquid crystal by using the 2 column-1 row method (see Fig. 8).

In the above description, we assumed that there is no coupling capacitance Cdd between the sub-pixel electrodes adjacent to each other. In practical, however, the coupling capacitance Cdd is in existence. A potential of each sub-pixel electrode will be described in the paragraphs that follow with a consideration of the coupling capacitance Cdd in addition to the capacitance Cgd, Cs, and Clc.

Fig. 4 shows a potential waveform of the sub-pixel electrode En in consideration of the coupling capacitance Cdd. In Fig. 4, furthermore, the potential waveforms (1), (2), which are selected from the potential waveforms (1), (2), and (3) of Fig. 3 obtained in the absence of the coupling capacitance, are shown for the purpose of facilitating the understanding the difference between the potential waveforms in the presence or absence of the coupling capacitance Cdd.

Considering the coupling capacitance, we can draw the following equation.

$$Ct(i) = Cgd(i) + Cs(i) + Clc(i) + Cdd(i) + Cdd(i+1)$$

Ct (i) is substantially constant in spite of the variations in the value of "i " (i.e., even though any sub-pixel is considered), so that Ct(i) can be simply referred to as Ct.

In consideration of the coupling capacitance Cdd, the potential waveform of the sub-pixel electrode En can be represented as (1)'. That is, the sub-pixel electrode En receives the influence of the coupling capacitance Cdd (n + 1) (see Fig. 2), so that the positive writing potential does not become V (+) but it becomes V (+) + ΔVdd and the negative writing potential does not become V(-) but it becomes V(-) – ΔVdd. In the

following description, we will give reasons why such changes are occurred. However, for the sake of simplicity, when the potential of the sub-pixel electrodes En is considered, we assume that only the coupling capacitance Cdd (n + 1) of the coupling capacitance Cdd(i) is present and that the other coupling capacitances Cdd are disregarded. By the way, the coupling capacitance Cdd (n + 1) is the coupling capacitance between the sub-pixel electrode En and the sub-pixel electrode En+1.

The potential waveform (1)' in consideration of the coupling capacitance can be explained just as in the case of disregarding the coupling capacitance as described above up to the time t2. Now, attention must be directed toward the potential waveform (2) of the sub-pixel electrode En+1 which is subsequent to the sub-pixel electrode En. At the time t2 (i.e., at the time that the potential V(n) of the sub-pixel electrode En becomes V(+)), the potential V (n+1) of the sub-pixel electrode En+1 is a negative writing potential V(-). After a lapse of one horizontal period from the time t2 (i.e, at the time t3), the potential of the sub-pixel electrode En+1 changes from the negative writing potential V (-) to the positive writing potential V (+) since the sub-pixel R (n) and the sub-pixel R (n+1) are driven with the same polarity. By the way, the coupling capacitance Cdd is present between the sub-pixel electrode En and the sub-pixel electrode En+1. Therefore, when the potential of the sub-pixel electrode En+1 changes from the negative writing potential V (-) to the positive writing potential V (+), the positive writing potential Vp (n) of the sub-pixel electrode En can be expressed by the following equation in consideration of the law of conservation of charge with respect to the sub-pixel R (n).

$$Vp(n) = V(+) + \{(V(+) - V(-)\} \times Cdd/Ct$$
$$= V(+) + \{(Vsp - \Delta Vc) - (Vsn - \Delta Vc)\} \times Cdd/Ct$$
$$= V(+) + (Vsp - Vsn) \times Cdd/Ct$$

This expression gives us the fact that Vp (n) cannot be expressed simply as V (+) because it is influenced by the potential changes in the subsequent sub-pixel electrode En+1. That is to say, Vp(n) changes by the amount corresponding to the second term on the right side of the equation, i.e, (Vsp – Vsn) x Cdd/Ct. If this second term of the equation is replaced as the following equation (6), we obtain the equation (7) as follows.

$$\Delta Vdd = (Vsp - Vsn) \times Cdd/Ct \quad .....(6)$$
$$Vp(n) = V(+) + \Delta Vdd \quad .....(7)$$

Therefore, the positive writing potential Vp (n) of the sub-pixel electrode En is V (+) without consideration of the coupling capacitance (see the potential waveform (1)), while it is ΔVdd larger than V(+) in consideration of the coupling capacitance.

Furthermore, if the pulse P2 is generated in the gate bus Gn–1, a potential with an amplitude of "A" that corresponds to the pulse P2 is appeared in the potential waveform (1)' of the sub-pixel electrode En. Subsequently, if the pulse P2 is generated in the gate bus Gn, the TFT (n) becomes the ON state during the only time corresponding to a pulse width of the pulse P2. Consequently, a negative potential Vsn is supplied from the source bus S to the sub-pixel electrode En via the TFT (n). During the period K2 where the pulse P2 of the gate bus Gn is generating, therefore, the potential Vsn is written in the sub-pixel electrode En (at the time t6). However, the potential of the sub-pixel electrode En falls down by the kickbag amount ΔVc, so that it temporarily becomes $V(-) = Vsn - \Delta Vc$ (at the time t6). Now, attention must be directed toward the potential waveform (2) of the sub-pixel electrode En+1 which is subsequent to the sub-pixel electrode En. At the time t6 (i.e., at the time that the potential V(n) of the sub-pixel electrode En becomes V(-)), the potential V (n+1) of the sub-pixel electrode En+1 is a positive writing potential V(+). After a lapse of one horizontal period from the time t6 (i.e, at the time t7), the potential of the sub-pixel electrode En+1 changes from the positive writing potential V(+) to the negative writing potential V(-) since the sub-pixel R(n) and the sub-pixel R(n+1) are driven with the same polarity. By the way, the coupling capacitance Cdd is present between the sub-pixel electrode En and the sub-pixel electrode En+1. Therefore, when the potential of the sub-pixel electrode En+1 changes from the positive writing potential V(+) to the negative writing potential V(-), the negative writing potential Vn(n) of the sub-pixel electrode En can be expressed by the following equation in consideration of the law of conservation of charge with respect to the sub-pixel R(n).

$$
\begin{aligned}
&Vn(n)\\
&= V(-) + \{(V(-) - V(+)\} \times Cdd/Ct\\
&= V(-) + \{(Vsn - \Delta Vc) - (Vsp - \Delta Vc)\} \times Cdd/Ct\\
&= V(-) + (Vsn - Vsp) \times Cdd/Ct\\
&= V(-) - (Vsp - Vsn) \times Cdd/Ct
\end{aligned}
$$

This expression gives us the fact that Vn(n) cannot be expressed simply as V(-) because it is influenced by the potential changes in the subsequent sub-pixel electrode En+1. That is to say, Vn(n) changes by the amount corresponding to the second term on the right side of the equation, i.e, (Vsp – Vsn) x Cdd/Ct. If this second term of the equation is replaced just as in the case of the equation (7), we obtain the equation (8) as follows.

$$Vn(n) = V(-) - \Delta Vdd \qquad .....(8)$$

Therefore, the negative writing potential Vn(n) of the sub-pixel electrode En is V(-) without consideration of the coupling capacitance (see the potential waveform (1)),

while it is ΔVdd smaller than V(-) in consideration of the coupling capacitance. Consequently, the potential difference between the positive writing potential V(+) + ΔVdd = Vsn – ΔVc – ΔVdd and the negative writing potential V(-) – ΔVdd = Vsn – ΔVc – ΔVdd is expressed by the following equation.

Vsp – Vsn + 2ΔVdd = Va + 2ΔVdd (see the equation (5))

Next, we will consider that a potential waveform of the sub-pixel electrode En+1 in the consideration of the coupling capacitance Cdd.

Fig. 5 shows a potential waveform of the sub-pixel electrode En+1 in consideration of the coupling capacitance Cdd. In Fig. 5, furthermore, the potential waveforms (2), (3), which are selected from the potential waveforms (1), (2), and (3) of Fig. 3 obtained in the absence of the coupling capacitance, are shown for the purpose of facilitating the understanding the difference between the potential waveforms in the presence or absence of the coupling capacitance Cdd.

In consideration of the coupling capacitance Cdd, the potential waveform of the sub-pixel electrode En+1 can be represented as (2)'. That is, the sub-pixel electrode En+1 receives the influence of the coupling capacitance Cdd (n+2) (see Fig. 2), so that the positive writing potential does not become V(+) but it becomes V(+) - ΔVdd and the negative writing potential does not become V(-) but it becomes V(-) + ΔVdd. In the following description, we will give reasons why such changes are occurred. However, for the sake of simplicity, when the potential of the sub-pixel electrodes En+1 is considered, we assume that only the coupling capacitance Cdd (n+1) of the coupling capacitance Cdd(i) is present and that the other coupling capacitances Cdd are disregarded. Herein, the coupling capacitance Cdd (n+2) is the coupling capacitance between the sub-pixel electrode En+1 and the sub-pixel electrode En+2.

The potential waveform (2)' in consideration of the coupling capacitance can be explained just as in the case of disregarding the coupling capacitance as described above up to the time t3. Now, attention must be directed toward the potential waveform (3) of the sub-pixel electrode En+2 which is subsequent to the sub-pixel electrode En+1. At the time t3 (i.e., at the time that the potential V(n+1) of the sub-pixel electrode En+1 becomes V(+)), the potential V (n+2) of the sub-pixel electrode En+2 is a positive writing potential V(+). After a lapse of one horizontal period from the time t3 (i.e, at the time t4), the potential of the sub-pixel electrode En+2 changes from the positive writing potential V (+) to the negative writing potential V (-) since the sub-pixel R (n+1) and the sub-pixel R (n+2) are driven with the opposite polarities. By the way, the coupling capacitance Cdd is present between the sub-

pixel electrode En+1 and the sub-pixel electrode En+2. Therefore, when the potential of the sub-pixel electrode En+2 changes from the positive writing potential V (+) to the negative writing potential V (-), the positive writing potential Vp (n+1) of the sub-pixel electrode En+1 can be expressed by the following equation in consideration of the law of conservation of charge with respect to the sub-pixel R (n+1).

$$
\begin{aligned}
&Vp\,(n+1)\\
&= V\,(+) + \{(V(-) - V(+)\} \times Cdd/Ct\\
&= V\,(+) + \{(Vsn - \Delta Vc) - (Vsp - \Delta Vc)\} \times Cdd/Ct\\
&= V\,(+) + (Vsn - Vsp) \times Cdd/Ct\\
&= V\,(+) - (Vsp - Vsn) \times Cdd/Ct
\end{aligned}
$$

This expression gives us the fact that Vp (n+1) cannot be expressed simply as V (+) because it is influenced by the potential changes in the subsequent sub-pixel electrode En+2. That is to say, Vp(n+1) changes by the amount corresponding to the second term on the right side of the equation, i.e, (Vsp – Vsn) x Cdd/Ct. If this second term of the equation is replaced with ΔVdd just as in the case of the equations (7) and (8), we obtain the equation (9) as follows.

$$Vp\,(n+1) = V\,(+) - \Delta Vdd \qquad .....(9)$$

Therefore, the positive writing potential of the sub-pixel electrode En+1 is V (+) without consideration of the coupling capacitance (see the potential waveform (2)), while it is ΔVdd smaller than V(+) in consideration of the coupling capacitance.

Furthermore, if the pulse P2 is generated in the gate bus Gn, a potential with an amplitude of "A" that corresponds to the pulse P2 is appeared in the potential waveform (2)' of the sub-pixel electrode En+1. Subsequently, if the pulse P2 is generated in the gate bus Gn+1, the TFT (n+1) becomes the ON state during the only time corresponding to a pulse width of the pulse P2. Consequently, a negative potential Vsn is supplied from the source bus S to the sub-pixel electrode En+1 via the TFT (n+1). During the period K4 where the pulse P2 of the gate bus Gn+1 is generating, therefore, the potential Vsn is written in the sub-pixel electrode En+1 (at the time t7). However, the potential of the sub-pixel electrode En+1 falls down by the kickbag amount ΔVc, so that it temporarily becomes V (-) = Vsn – ΔVc (at the time t7). Now, attention must be directed toward the potential waveform (3) of the sub-pixel electrode En+2 which is subsequent to the sub-pixel electrode En+1. At the time t7 (i.e., at the time that the potential V(n+1) of the sub-pixel electrode En+1 becomes V(-)), the potential V (n+2) of the sub-pixel electrode En+2 is a negative writing potential V(-). After a lapse of one horizontal period from the time t7 (i.e, at the time t8), the potential of the sub-pixel electrode En+2 changes from the negative writing potential V (-) to the

positive writing potential V (+) since the sub-pixel R (n+1) and the sub-pixel R (n+2) are driven with the opposite polarity. By the way, the coupling capacitance Cdd (see Fig.2)is present between the sub-pixel electrode En+1 and the sub-pixel electrode En+2. Therefore, when the potential of the sub-pixel electrode En+2 changes from the negative writing potential V(-) to the positive writing potential V(+), the negative writing potential Vn(n+1) of the sub-pixel electrode En+1 can be expressed by the following equation in consideration of the law of conservation of charge with respect to the sub-pixel R(n+1).

Vn(n+1)

$= V(-) + \{(V(+) - V(-)\} \times Cdd/Ct$

$= V(-) + \{(Vsp - \Delta Vc) - (Vsn - \Delta Vc)\} \times Cdd/Ct$

$= V(-) + (Vsp - Vsn) \times Cdd/Ct$

This expression gives us the fact that Vn(n+1) cannot be expressed simply as V(-) because it is influenced by the potential changes in the subsequent sub-pixel electrode En+2. That is to say, Vn(n+1) changes by the amount corresponding to the second term on the right side of the equation, i.e, (Vsp – Vsn) x Cdd/Ct. If this second term of the equation is replaced just as in the case of the equation (7), we obtain the equation (10) as follows.

$$Vn\ (n+1) = V\ (-) + \Delta Vdd \qquad .....(10)$$

Therefore, the negative writing potential Vn(n+1) of the sub-pixel electrode En+1 is V(-) without consideration of the coupling capacitance (see the potential waveform (2)), while it is ΔVdd larger than V(-) in consideration of the coupling capacitance. Consequently, the potential difference between the positive writing potential V(+) - ΔVdd = Vsp – ΔVc – ΔVdd and the negative writing potential V(-) – ΔVdd = Vsn – ΔVc + ΔVdd is expressed by the following equation.

$Vsp - Vsn - 2\Delta Vdd = Va - 2\Delta Vdd$ (see the equation (5))

As described above, the positive and negative writing potentials of the sub-pixel electrode are effected by the coupling capacitance. As a result, we can recognize that the positive and negative writing potentials are changed by an amount of ΔVdd in comparison with those potentials without consideration of the coupling capacitance. This can be summarized as follows;

Firstly, we focus on one sub-pixel electrode. If a potential of the sub pixel electrode subsequent to the focused sub-pixel electrode changes from a negative writing potential to positive writing potential immediately after a potential is written into the focused sub-pixel electrode, the potential of the focused sub pixel electrode increases by an amount of ΔVdd. On the other hand, if a potential of the sub pixel electrode subsequent to the focused

sub-pixel electrode changes from a positive writing potential to negative writing potential immediately after a potential is written into the focused sub-pixel electrode, conversely, the potential of the focused sub pixel electrode decreases by an amount of ΔVdd. Considering such a fact, the positive writing potential of the sub-pixel electrode R(n+2) in consideration of the coupling capacitance is ΔVdd smaller than the positive writing potential of the same sub-pixel electrode R(n+2) without consideration of the coupling capacitance, since the sub-pixel electrode R(n+3) subsequent to the sub-pixel electrode R(n+2) is changed from the positive writing potential to the negative writing potential immediately after a potential is written into the sub-pixel electrode R(n+2). On the other hand, the negative writing potential of the sub-pixel electrode R(n+2) in consideration of the coupling capacitance is ΔVdd larger than the positive writing potential of the same sub-pixel electrode R(n+2) without consideration of the coupling capacitance, since the sub-pixel electrode R(n+3) subsequent to the sub-pixel electrode R(n+2) is changed from the negative writing potential to the positive writing potential.

Fig. 6 shows a potential waveform of the sub-pixel electrode En, En+1 and En+2 in consideration of the coupling capacitance Cdd. In Fig. 6, furthermore, the potential waveform (1) of the sub-pixel electrode En without consideration of the coupling capacitance is also shown.

In Fig. 6, as example of potential waveforms in consideration of the coupling capacitance Cdd, potential waveforms of only three sub-pixel electrodes En, En+1, and En+2 are shown. However, we can find it on the basis of the explanation with reference to Figs. 4 and 5 that each of the positive and negative writing potentials of the other sub-pixel electrodes decrease or increase by an amount of ΔVdd. Therefore, the positive writing potential Vp(i) and the negative writing potential Vn(i) of each sub-pixel R(i) can be expressed by the following equations (11) to (14).

$$Vp(i) = V(+) + \Delta Vdd = Vsp - \Delta Vc + \Delta Vdd \quad ....(11)$$

where i = n, n±2, n±4, ...

$$Vp(i) = V(+) - \Delta Vdd = Vsp - \Delta Vc - \Delta Vdd \quad ....(12)$$

where i = n±1, n±3, ...

$$Vn(i) = V(-) - \Delta Vdd = Vsn - \Delta Vc - \Delta Vdd \quad ....(13)$$

where i = n, n±2, n±4, ...

$$Vn(i) = V(-) + \Delta Vdd = Vsn - \Delta Vc + \Delta Vdd \quad ....(14)$$

where i = n±1, n±3, ...

Furthermore, if the coupling capacitance is neglected, as shown in Fig. 3, the writing potential difference of each sub-pixel becomes Va, so that it is constant regardless of the sub-pixels. If the coupling capacitance is considered, on the other hand, we can find it from the above equations (11) to (14) that there are two different writing potential differences, one is $2\Delta Vdd$ larger than Va and the other is $2\Delta Vdd$ smaller than Va, are generated alternately. In the above description, only one source bus is considered. However, the phenomenon of fluctuations in the writing potential difference by an amount of $2\Delta Vdd$ can be observed with respect to all source buses. Therefore, if the liquid crystal is a normally white panel, a line on which the writing potential difference is $2\Delta Vdd$ larger than Va becomes dark while the writing potential difference is $2\Delta Vdd$ smaller than Va becomes bright. In the conventional liquid crystal display device, user recognizes the horizontal stripes where light column and dark column occur alternately in spite of trying to equalize the lightness among the sub-pixels.

In the liquid crystal display device shown in Fig. 1, on the other hand, a potential generation circuit 5 comprises a positive correction part 52 and a negative correction part 54. If an image to be represented by the uniform lightness (i.e, an image of blue sky) is displayed by using the liquid crystal display device shown in Fig. 1 comprising the correction parts 52 and 54, the blue sky can be displayed by uniform lightness without light and dark patterns on the whole screen. We can explain this reasons as follows.

Fig. 7 is a timing chart showing the timing when the potentials are applied to the respective sub-pixel electrodes En, En + 1, and En + 2.

The cause of horizontal stripes where light column and dark column occur alternately may be considered as follows. That is, one of sub-pixel electrodes adjacent to each other has a writing potential difference which is $2\Delta Vdd$ larger than Va and the other has a writing potential difference which is $2\Delta Vdd$ smaller than Va, so that different voltages are applied on the sub-pixel electrodes, respectively. Therefore, the horizontal stripes can be prevented by equally applying voltages on the respective sub-pixels if the difference between the potential Vcom of the common electrode and the positive writing potential becomes equal regardless of the sub-pixels and the difference between the potential Vcom of the common electrode and the negative writing potential also becomes equal regardless of the sub-pixels.

In the conventional liquid crystal display as described above with reference to Fig. 3, potentials Vsp are evenly written on the respective sub-pixels in order to equalize positive writing potentials of the respective sub-pixel electrodes, on the other hand, potentials Vsn are evenly written on the respective sub-pixels in order to equalize negative writing

potentials of the respective sub-pixel electrode. However, the positive and negative writing potentials of each sub-pixel electrode are influenced by the coupling capacitance, so that these potentials are varied with an amount of ΔVdd in comparison with those of each sub-pixel electrode without consideration of the coupling capacitance. As a result, the difference between the positive or negative writing potential and the potential Vcom of the common electrodes is varied among the sub-pixels.

If the coupling capacitance is considered in the conventional liquid crystal display device, two types of the positive writing potentials, i.e, V(+) + ΔVdd and V(+) - ΔVdd, are appeared. Further, two types of the negative writing potentials, i.e, V(-) + ΔVdd and V(-) - ΔVdd, are appeared. Now, if we focus attention to the positive writing potential, the difference between the two types of potentials, V(+) + ΔVdd and V(+) - ΔVdd, is 2ΔVdd. Therefore, if the potential of the sub-pixel electrode where the potential V(+) + ΔVdd is appeared can be decreased by an amount of ΔVdd, and further, if the potential of the sub-pixel electrode where the potential V(+) - ΔVdd is appeared can be increased by an amount of ΔVdd, the positive writing potentials of all sub-pixel electrode becomes V(+), so that, the differences between the potential Vcom of the common electrode and each of the positive writing potentials of all sub-pixels become equal each other. Next, we focus attention to the negative writing potential. As in the case of positive writing potential, if the potential of the sub-pixel electrode where the potential V(-) + ΔVdd is appeared can be decreased by an amount of ΔVdd, and further, if the potential of the sub-pixel electrode where the potential V(-) - ΔVdd is appeared can be increased by an amount of ΔVdd, the negative writing potentials of all sub-pixel electrode becomes V(-), so that, the differences between the potential Vcom of the common electrode and each of the negative writing potential of all sub pixel electrodes become equal each other. That is, the potential of each sub-pixel electrode is decreased or increased by the amount of ΔVdd. Therefore, the correction may be performed by the amount ΔVdd.

According to the present embodiment, in order to correct a signal waveform of the source bus S to a waveform shown in Fig. 7, a potential generation circuit 5 has a positive correction part 52 and a negative correction part 54 as shown in Fig. 1. The correction of the potential waveform is performed as follows; Among the sub-pixel electrodes, attention is directed toward sub-pixel electrodes Ei (where i = n, n±2, n±4, ...) (hereinafter, referred to as first sub-pixel electrodes) of which the writing potential difference in consideration of the coupling capacitance is Va + 2ΔVdd if the conventional source bus signal (e.g., see Fig. 6) is applied. In the period where the positive potentials is written on the first sub-pixel electrodes

(which period corresponds to the period of K1 or K6 in Fig. 7), the potential of source bus S is corrected to the potential Vsp(-) which is smaller than Vsp by ΔVdd (i.e., Vsp(-) = Vsp - ΔVdd). On the other hand, in the period where the negative potentials is written on the first sub-pixel electrodes (which period corresponds to the period of K2 or K5 in Fig. 7), the potential of source bus S is corrected to the potential Vsn(+) which is larger than Vsn by ΔVdd (i.e., Vsn(+) = Vsn + ΔVdd).

Further, among the sub-pixel electrodes, attention is directed toward sub-pixel electrodes Ei (where i = n±1, n±3, ...) (hereinafter, referred to as second sub-pixel electrodes) of which the writing potential difference is Va - 2ΔVdd if the conventional source bus signal is used. In the period where the positive potentials is written on the second sub-pixel electrodes (which period corresponds to the period of K3 in Fig. 7), the potential of source bus S is corrected to the potential Vsp(+) which is larger than Vsp by ΔVdd (i.e., Vsp(+) = Vsp + ΔVdd). On the other hand, in the period where the negative potentials is written on the second sub-pixel electrodes (which period corresponds to the period of K4 in Fig. 7), the potential of source bus S is corrected to the potential Vsn(-) which is smaller than Vsn by ΔVdd (i.e., Vsn(-) = Vsn - ΔVdd).

In order to correct the potentials of the source bus S to each of the potentials Vsp(-) and Vsp(+) during the period where the positive potential is written on each of the first and second sub-pixel electrodes, the positive correction part 52 generates rectangular signals to be required to correct the potentials of the source bus S from Vsp to each of the Vsp (-) and Vsp (+). Furthermore, in order to correct the potentials of the source bus S to each of the Vsn(+) and Vsn(-) during the period where the negative potential is written on each of the first and second sub-pixel electrodes, the negative correction part 54 generates rectangular signals to be required to correct the potential of the source bus S from Vsn to each of Vsn(+) and Vsn(-).

In the present embodiment, since the potential of the source bus S is corrected by the signals generated from the positive and negative correction parts 52, 54 as described above, the positive writing potential Vp1 of the first sub-pixel electrode can be obtained by replacing Vsp with Vsp(-) = Vsp - ΔVdd in the equation (11) and performing the calculation of the replaced equation (11). That is, the Vp1 can be expressed by the following equation.

Vp1 = (Vsp - ΔVdd) – ΔVc + ΔVdd = Vsp – ΔVc = V(+) (see the equation (2)).

Furthermore, the positive writing potential Vp2 of the second sub-pixel electrode can be obtained by replacing Vsp with Vsp(+) = Vsp + ΔVdd in the equation (12) and performing the calculation of the replaced equation (12).

That is, Vp2 = (Vsp + ΔVdd) - ΔVc - ΔVdd = Vsp - ΔVc = V(+) (see the equation (2)).

In the present embodiment, therefore, it is recognized that the positive writing potential of each sub-pixel electrode becomes V(+). Therefore, the voltages applied to all sub-pixels becomes V(+) – Vcom at the positive time.

Next, in the present embodiment, we consider about the negative writing potential Vn. The negative writing potential Vn1 of the first sub-pixel electrode can be obtained by replacing Vsn with Vsn(+) = Vsn + ΔVdd in the equation (13) and performing the calculation of the replaced equation (13). That is, the Vn1 can be expressed by the following equation.

Vn1 = (Vsn + ΔVdd) – ΔVc - ΔVdd = Vsn – ΔVc = V(-) (see the equation (3)).

The negative writing potential Vn2 of the second sub-pixel electrode can be obtained by replacing Vsn with Vsn(-) = Vsn - ΔVdd in the equation (14) and performing the calculation of the replaced equation (14). That is, the Vn2 can be expressed by the following equation.

Vn2 = (Vsn - ΔVdd) – ΔVc + ΔVdd = Vsn – ΔVc = V(-) (see the equation (3)).

In the present embodiment, therefore, it is recognized that the negative writing potential of each sub-pixel electrode becomes V(-). Therefore, the voltages applied to all sub-pixels becomes Vcom - V(-) at the negative time. Consequently, the writing potential difference becomes V(+) – V(-) = Vsp - ΔVc – (Vnp - ΔVc) = Vsp – Vnp = Va (see the equation (5)).

In addition, as indicated in the equation (4), Vcom is defined as (Vsp + Vsn)/2 - ΔVc. Therefore, there is a relationship expressed by the following equation.

V(+) – Vcom (= voltage applied to each sub-pixel at the positive time) = Vcom – V (-) (= voltage applied to each sub-pixel at the negative time)

Therefore, if an image to be represented by the uniform lightness (i.e, an image of blue sky) is displayed by using the liquid crystal display device shown in Fig. 1, the blue sky can be displayed by uniform lightness without light and dark patterns on the whole screen.

In the above description, furthermore, we consider the example for rendering all the sub-pixels the same lightness. Therefore, for all sub-pixel electrodes, the correction amount ΔVdd of the potential of the source bus S can be defined to a predetermined constant value calculated by using equation (6). In general, however, the lightness of each sub-pixel is varied in multiple levels (e.g., 64 levels). Therefore, Vs and Vn in the equation (6) is inherently varied. That is, ΔVdd in the equation (6) is also varied. For example, if the liquid crystal display device of a normally white mode is considered, the writing potential deference

is more enlarged while the sub-pixel is more darkened, resulting in the increase in ΔVdd. On the other hand, the lightness of the sub-pixel is more increased while the writing potential deference is more decreased, resulting in the decrease in ΔVdd. ΔVdd in the equation (6) is a variation amount of the positive and negative writing potentials of each sub-pixel electrode, which variation amount is caused by the writing potential difference of the subsequent (next line) sub-pixel electrode. Therefore, the correction amount ΔVdd corresponding to each sub-pixel may be varied in response to the brightness of the subsequent sub-pixels.

In the present embodiment, furthermore, but not limited to, two different correction parts (i.e., positive and negative correction parts 52, 54) are provided. Only one of both correction parts can be used when ΔVdd is several tens of mV. If only one correction part is provided, the center voltages at alternation driving about the sub-pixels adjacent to each other in the direction of extending the source bus S (see Fig. 2) are deviated from each other. However, such a deviation can be neglected because of considering the deviation of the potential Vcom of the common electrode in a panel surface.

Considering the voltage-light transmission characteristics of the liquid crystal, the extent of variations in the light transmission with respect to the extent of variations in voltage is large at a region corresponding to a halftone. However, the extent is small at a region close to the side of white or black. Therefore, even if a signal to be generated from positive correction part 52 is added not from input part of the amplifier 55 but from the ladder resistance R1 to R4, the substantially same waveform as the corrected waveform (shown in Fig.7) of source bus S is obtained as long as the addition position is near the position where the reference potentials V1, V5 are generated. In the present embodiment, therefore, signals to be generated from the positive correction part 52 are added before the supply voltage from the power supply 51 is dividing by resistance, but not limited to. It is also possible that these signals are added from the ladder resistances R1 to R4. Likewise, signals to be generated from the negative correction part 54 may be added from the ladder resistances R6 to R10 as long as the addition position is near the positions where the reference potentials V6, V10 are generated.

In the present embodiment, furthermore, the liquid crystal display device comprises both the positive and negative correction parts 52, 54. These correction parts 52, 54 are responsible for preventing the generation of horizontal stripes by correcting the potential of the source bus S with a predetermined amount of the correction on the basis of the coupling capacity. Alternatively, data correction means for correcting a plurality of sub-pixel on the basis of the coupling capacitance may be provided instead of the correction parts

described above. The generation of horizontal stripes may be prevented by selecting each of potentials corresponding to a plurality of pixel data which had already corrected by the data correction means and supplying the selected potential to the source bus S.

The liquid crystal display device of the present embodiment adopts 2 column-1 row method as a driving method. According to the present invention, it is not limited to such a method, it is also possible to adopt other driving methods. One of such methods is 3 column-1 row method. The variations in the voltage of each sub-pixel by the coupling capacitance formed between the adjacent sub-pixels is prevented by the present invention.

In the present embodiment, but not limited to, the liquid crystal display device is in the type of displaying a color image. However, the liquid crystal display device according to the present invention can be applied to a black-and-white display device, in order to effectively prevent the generation of horizontal stripes in the black-and-white display device.

In the present embodiment, but not limited to, the reference potentials V1 to V10 are directly introduced into the DAC 3b. A buffer of an amplifier may be provided between the ladder resistances and each DAC 3b.

In the present embodiment, but not limited to, the potential Vcom of the common electrode is maintained at constant. According to the present invention, it is also possible to provide the potential Vcom as a variable.

According to the present invention, horizontal stripes are prevented even though the liquid crystal display device displays an image represented by a substantially constant lightness.

Fig. 1 is a block diagram that illustrates the configuration of a liquid crystal display device as one mode for carrying out the invention.

Fig. 2 is an enlarged view of a part of the TFT substrate of the liquid crystal panel 1 shown in Fig. 1.

Fig. 3 is a timing chart showing the timing when the potentials are applied to the respective sub-pixel electrodes En, En + 1, and En + 2.

Fig. 4 shows a potential waveform of the sub-pixel electrode En in consideration of the coupling capacitance Cdd.

Fig. 5 shows a potential waveform of the sub-pixel electrode En+1 in consideration of the coupling capacitance Cdd.

Fig. 6 shows a potential waveform of the sub-pixel electrode En, En+1 and En+2 in consideration of the coupling capacitance Cdd.

Fig. 7 is a timing chart showing the timing when the potentials are applied to the respective sub-pixel electrodes En, En + 1, and En + 2.

Fig.8 shows a conceptual rendering of 2 column-1 row method.

Reference Numeral

1 Liquid crystal panel

2 gate driver

3 source driver

3a,55,56 amplifier

3b DAC

3c latch

4 signal control unit and an power supply

5 gamma-correction reference potential generation circuit

51 positive-side electric power supply

52 signal generation part for correcting positive-side

53 negative-side electric power supply

54 signal generation part for correcting negative-side

CLAIMS:

1. A liquid crystal display device comprising:

a first substrate provided with plural pixel electrodes to which a potential is applied via a same data line;

a second substrate provided with a common electrode, liquid crystal being sandwiched between the first substrate and the second substrate; and

potential application means for applying the potential to the plural pixel electrodes on the basis of plural pixel data, and for correcting the potential to be applied to the plural pixel electrodes on the basis of coupling capacitances formed between mutually adjacent pixel electrodes.

2. The liquid crystal display device as claimed in claim 1, wherein the potential application means has reference potential generation means for generating reference potentials and reference potential correction means for correcting the reference potentials generated by the reference potential generation means on the basis of the coupling capacitances, and wherein the potential application means generates plural potentials from the corrected reference potentials, selects each of potentials corresponding to each of the plural pixel data from the plural potentials, and applies these selected potentials to the plural pixel electrodes.

3. The liquid crystal display device as claimed in claim 2, wherein the reference potential generation means generates plural reference potentials by a ladder resistance.

4. The liquid crystal display device as claimed in claim 3, wherein the reference potential correction means corrects the potential generated by the reference potential generation means at an intermediate position of the ladder resistance.

5. The liquid crystal display device as claimed in claim 1, wherein the potential application means has reference potential generation means for generating reference

potentials and data correction means for correcting the plural pixel data on the basis of the coupling capacitance,

the potential application means generates plural potentials from the corrected reference potentials, selects each of potentials corresponding to each of the corrected plural pixel data from the plural potentials, and applies these selected potentials to the plural pixel electrodes.

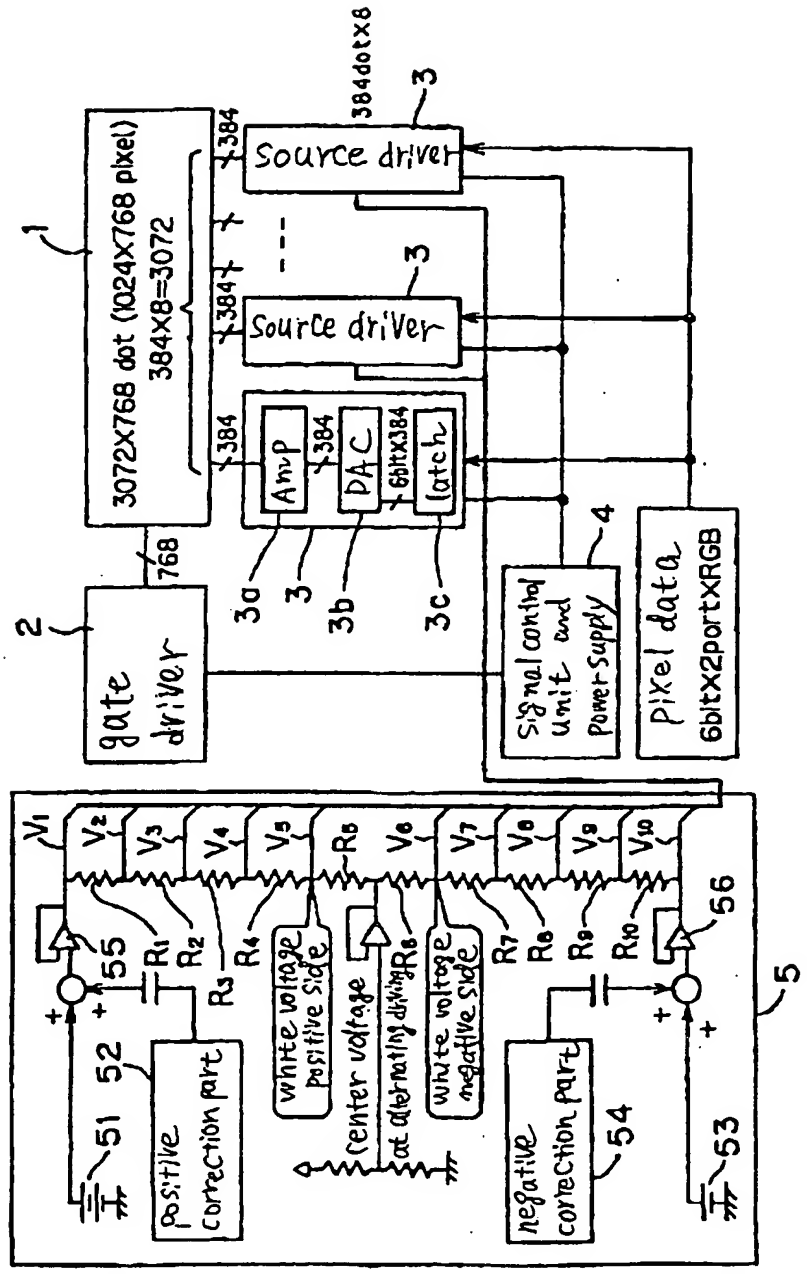
3072X768 dot (1024X768 pixel)
384X8=3072
1
384dotX8
3
Source driver
Source driver
384
Amp
DAC
6bitX384
latch
2
gate driver
768
3a
3
3b
3c
Signal control unit and Power Supply
4
Pixel data
6bitX2portXRGB
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
55
56
51
52
positive correction part
white voltage positive side
center voltage
at alternating driving
white voltage negative side
negative correction part
54
53
5

FIG. 1

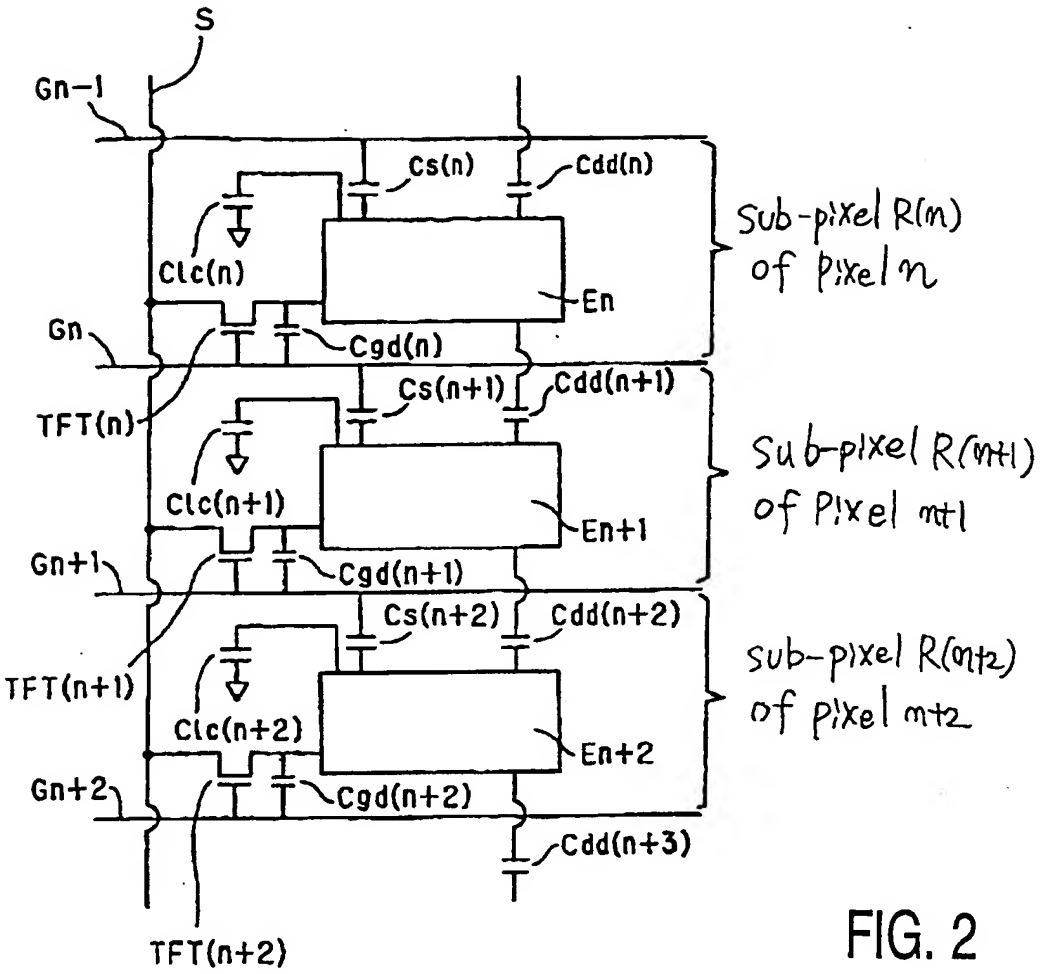
S
Gn-1
Cs(n)
Cdd(n)
Clc(n)
En
Gn
Cgd(n)
Sub-pixel R(n) of pixel n
Cs(n+1)
Cdd(n+1)
TFT(n)
Clc(n+1)
En+1
Gn+1
Cgd(n+1)
Sub-pixel R(n+1) of Pixel n+1
Cs(n+2)
Cdd(n+2)
TFT(n+1)
Clc(n+2)
En+2
Gn+2
Cgd(n+2)
sub-pixel R(n+2) of pixel n+2
Cdd(n+3)
TFT(n+2)

FIG. 2

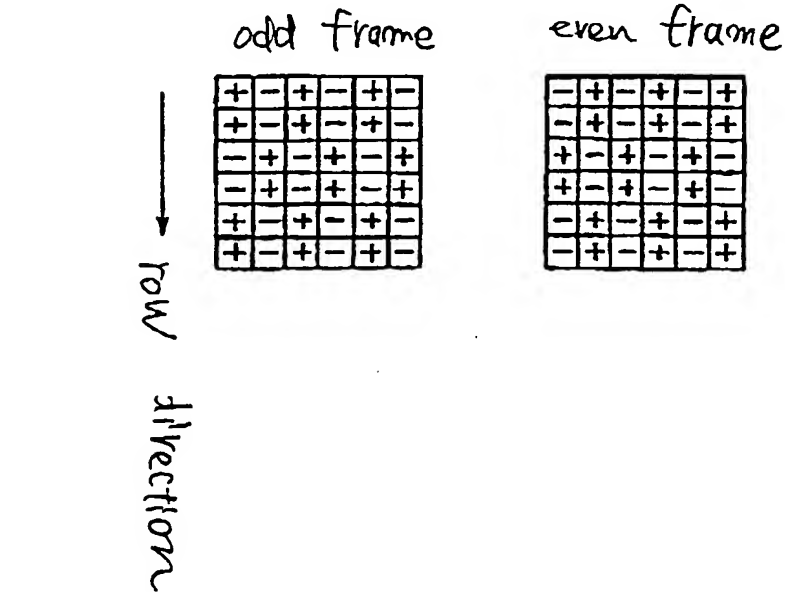
odd frame
even frame
row direction

FIG. 8

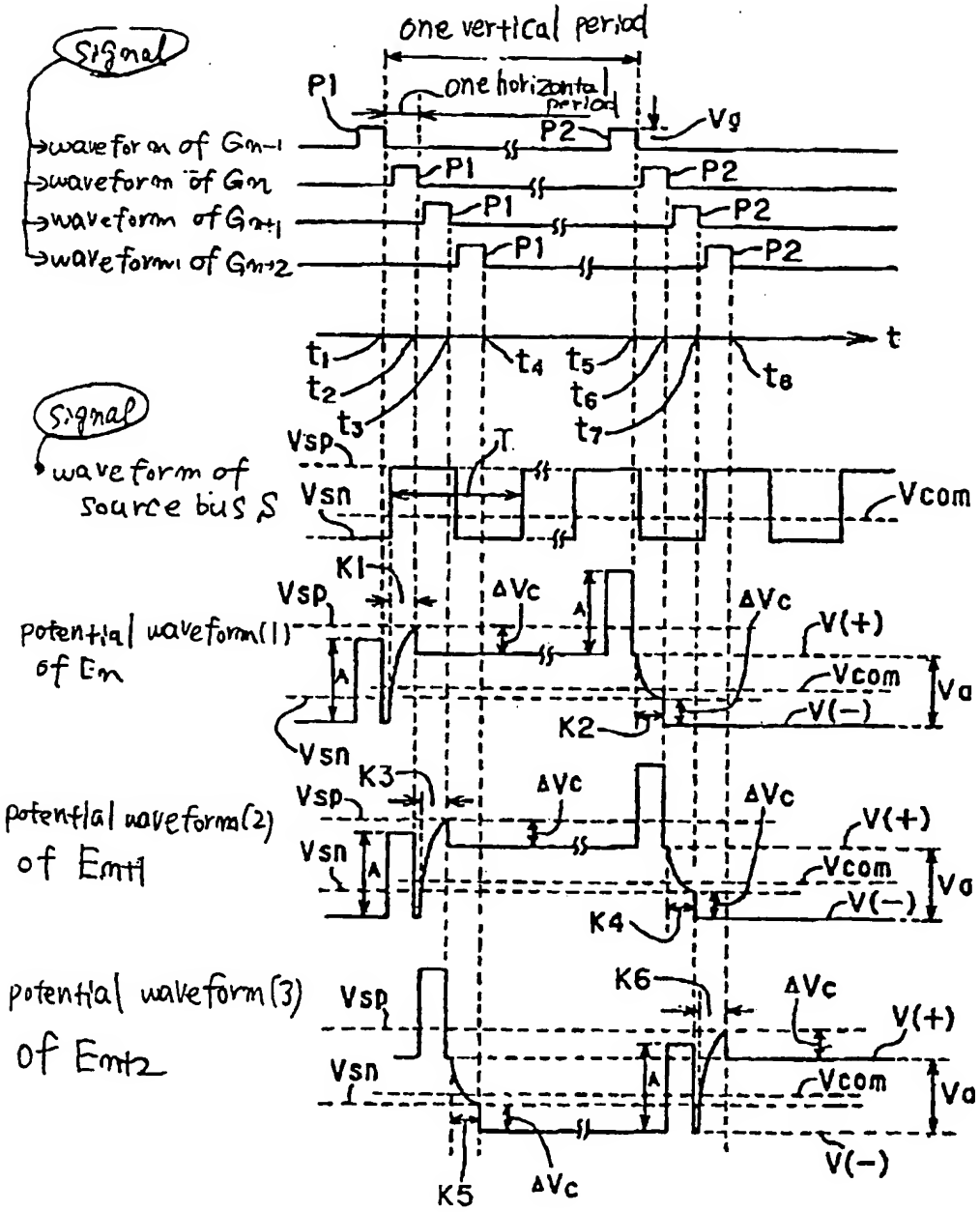
one vertical period
Signal
P1
one horizontal period
P2
Vg
waveform of Gn-1
waveform of Gn
waveform of Gn+1
waveform of Gn+2
t
t1
t2
t3
t4
t5
t6
t7
t8
Signal
waveform of source bus S
Vsp
Vsn
Vcom
K1
K2
K3
K4
K5
K6
ΔVc
A
V(+)
V(-)
Va
potential waveform(1) of Em
potential waveform(2) of Emt1
potential waveform(3) of Emt2

FIG. 3

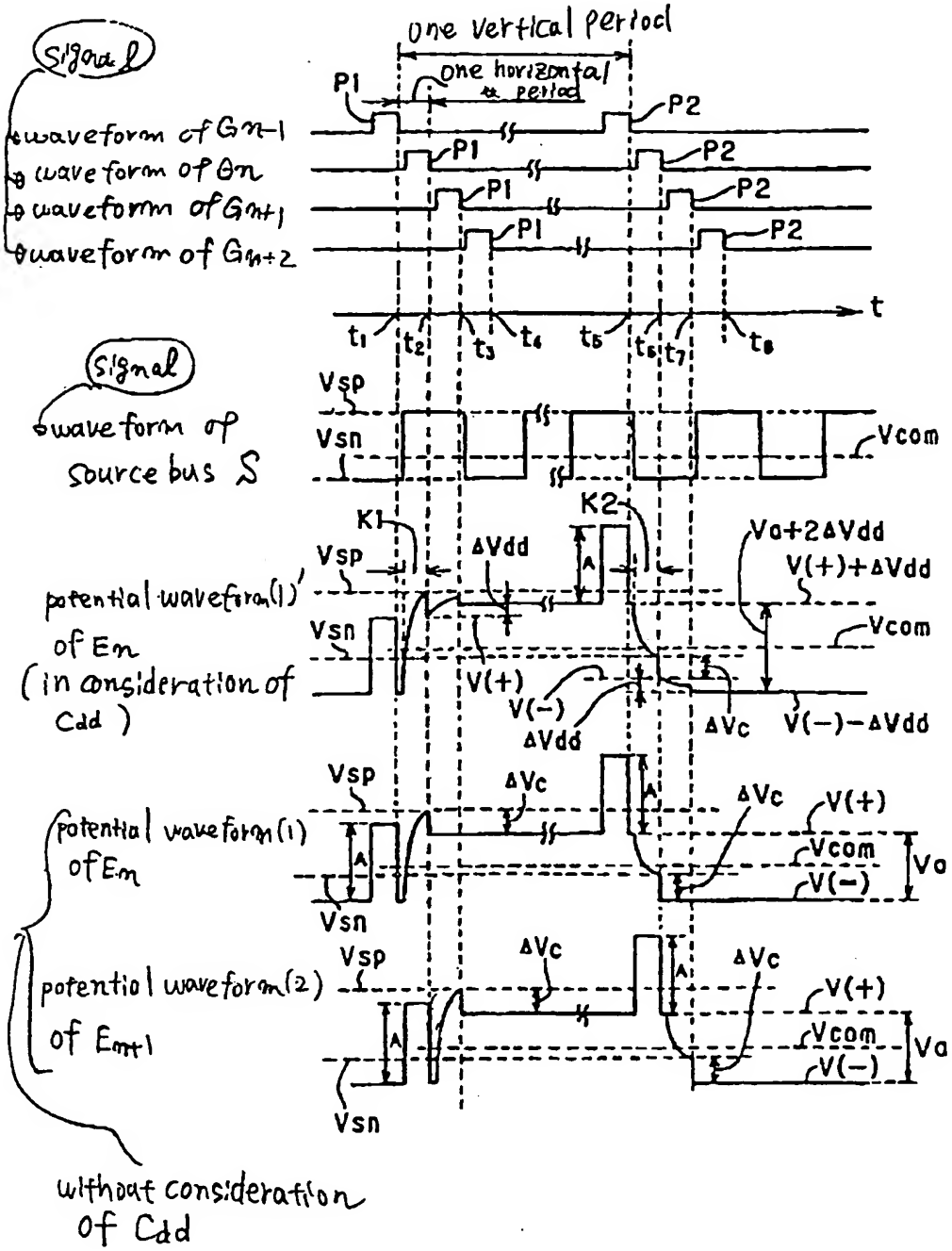
one vertical period
one horizontal period
Signal
waveform of Gn-1
waveform of Gn
waveform of Gn+1
waveform of Gn+2
P1
P2
t
t1 t2 t3 t4 t5 t6 t7 t8
Signal
waveform of source bus S
Vsp
Vsn
Vcom
K1
K2
ΔVdd
A
Vo+2ΔVdd
V(+)+ΔVdd
potential waveform(1)' of En (in consideration of Cdd)
V(+)
V(-)
ΔVdd
ΔVc
V(-)-ΔVdd
potential waveform(1) of En
potential waveform(2) of En+1
Vo
without consideration of Cdd

FIG. 4

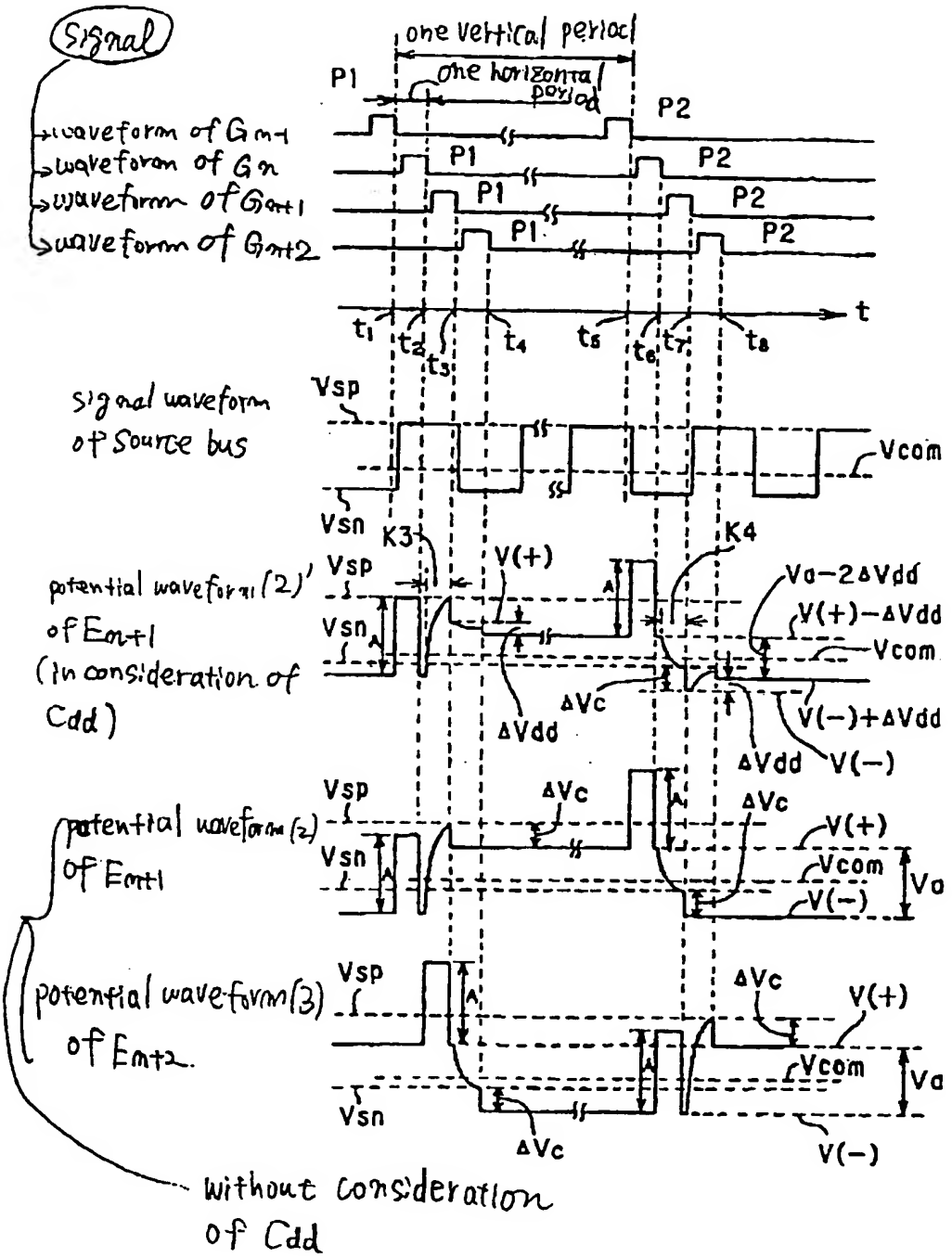
Signal
one vertical period
one horizontal period
P1
P2
waveform of Gm-1
waveform of Gm
waveform of Gm+1
waveform of Gm+2
t
t1
t2
t3
t4
t5
t6
t7
t8
signal waveform of Source bus
Vsp
Vsn
Vcom
K3
K4
potential waveform (2)' of Em+1 (In consideration of Cdd)
V(+)
Va-2ΔVdd
V(+)-ΔVdd
ΔVc
ΔVdd
V(-)+ΔVdd
V(-)
potential waveform (2) of Em+1
potential waveform (3) of Em+2
Va
without consideration of Cdd

FIG. 5

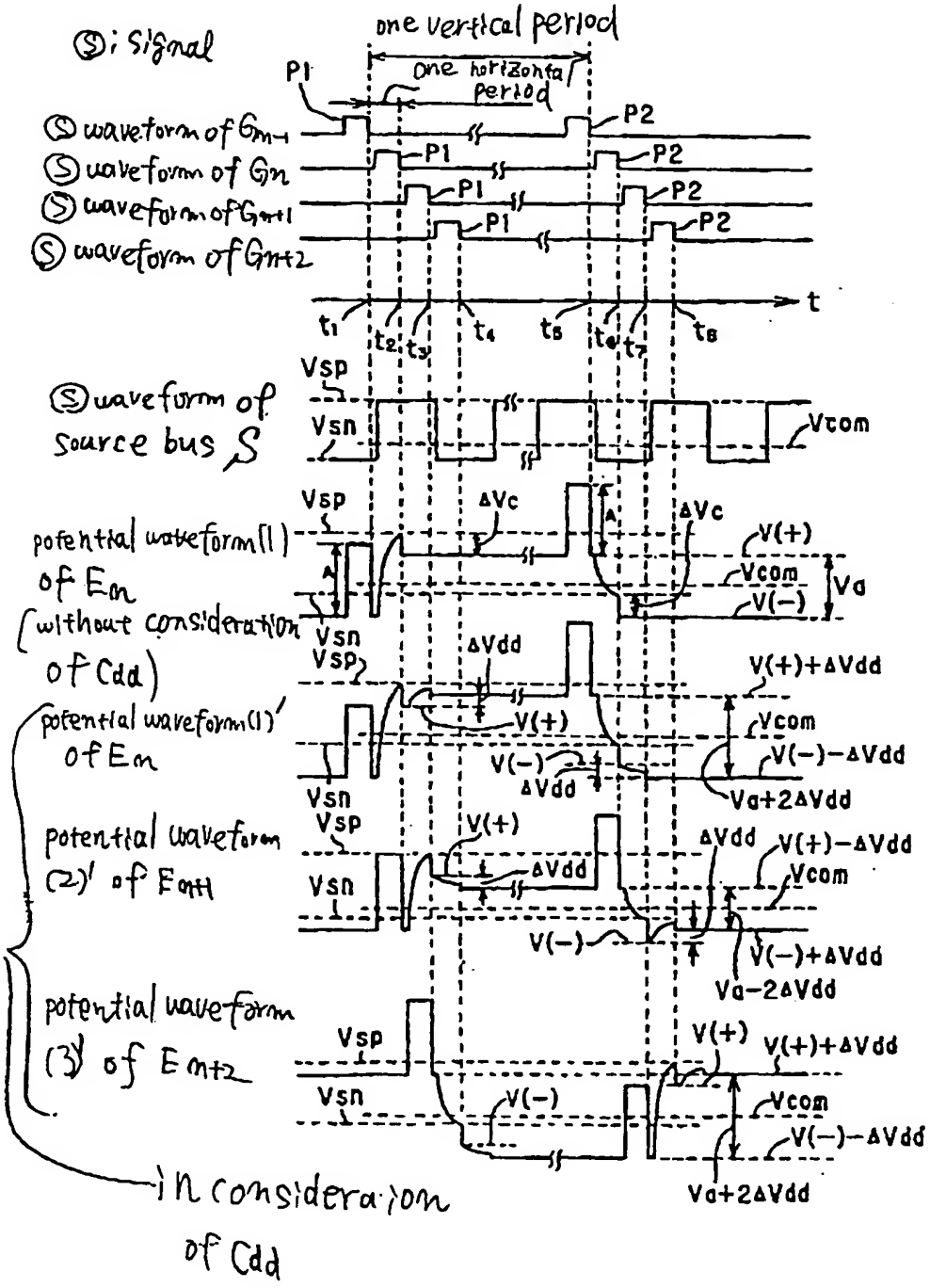
S: signal
one vertical period
one horizontal period
P1
P2
S waveform of Gn-1
S waveform of Gn
S waveform of Gn+1
S waveform of Gn+2
t
t1 t2 t3 t4 t5 t6 t7 t8
S waveform of source bus S
Vsp
Vsn
Vcom
potential waveform(1) of En (without consideration of Cdd)
ΔVc
V(+)
V(-)
Va
potential waveform(1)' of En
ΔVdd
V(+)+ΔVdd
V(-)-ΔVdd
Va+2ΔVdd
potential waveform (2)' of En+1
V(+)-ΔVdd
Va-2ΔVdd
potential waveform (3)' of En+2
in consideration of Cdd

FIG. 6

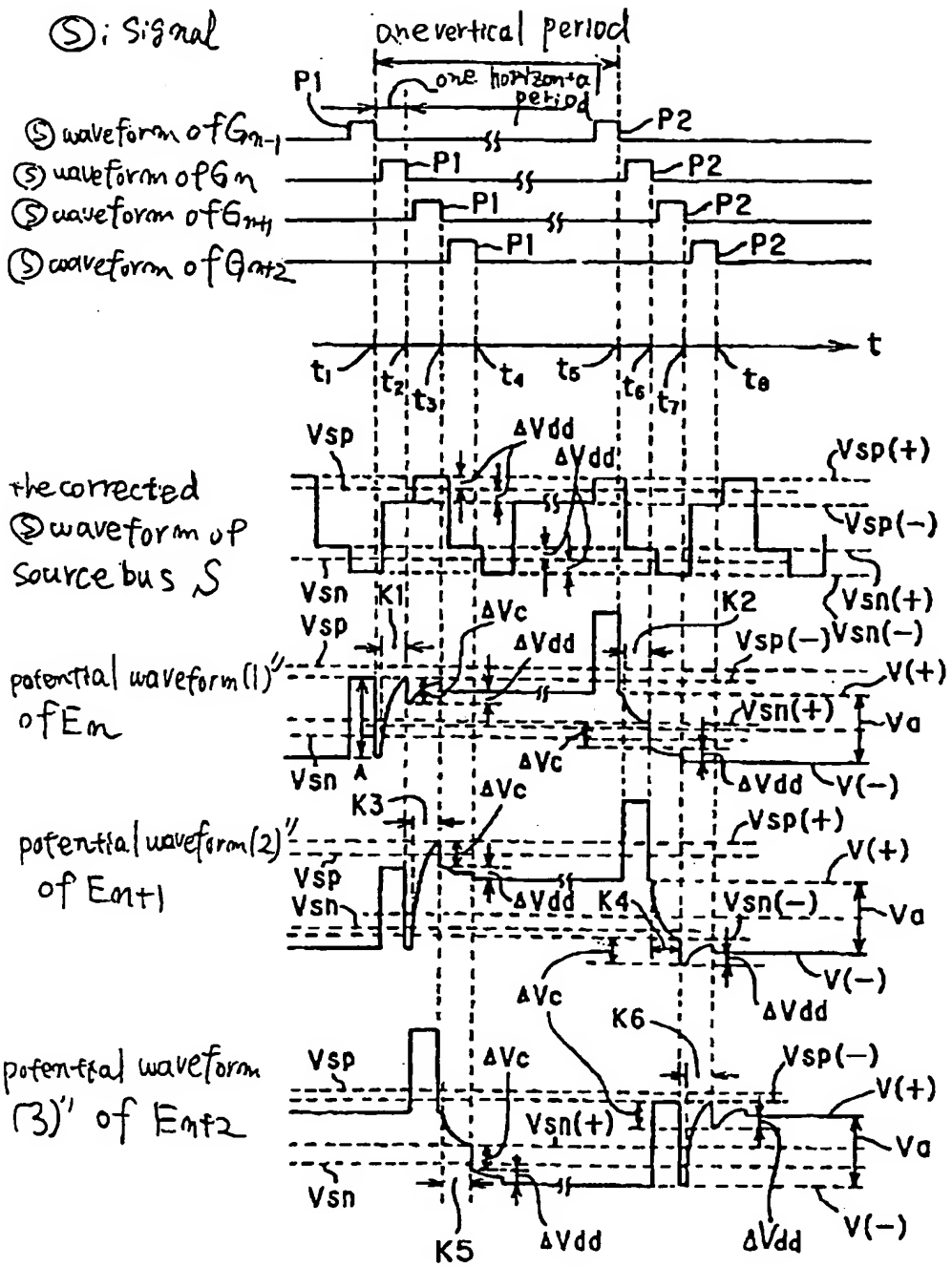
S: Signal
one vertical period
one horizontal period
P1
P2
S waveform of Gn-1
S waveform of Gn
S waveform of Gn+1
S waveform of Gn+2
t
t1
t2
t3
t4
t5
t6
t7
t8
the corrected S waveform of source bus S
Vsp
Vsn
ΔVdd
Vsp(+)
Vsp(-)
Vsn(+)
Vsn(-)
K1
K2
potential waveform (1)'' of En
ΔVc
V(+)
V(-)
Va
A
K3
potential waveform (2)'' of En+1
K4
potential waveform (3)'' of En+2
K5
K6

FIG. 7

INTERNATIONAL SEARCH REPORT

Inte...ational Application No
PCT/EP 00/09674

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 11, 30 September 1998 (1998-09-30) -& JP 10 171412 A (NEC CORP), 26 June 1998 (1998-06-26)	1-3,5
Y	abstract	4
X,P	-& US 6 075 507 A (HADA HIROSHI ET AL) 13 June 2000 (2000-06-13)	1-3,5
Y,P	see abstract column 1, line 9 - line 19 column 2, line 4 - line 14; figure 2 column 4, line 6 - line 53; figures 4,5 column 5, line 11 - line 56; figures 6,8	4

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search	Date of mailing of the international search report
26 February 2001	05/03/2001

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Int...ational Application No
PCT/EP 00/09674

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 02, 26 February 1999 (1999-02-26) -& JP 10 301538 A (SHARP CORP), 13 November 1998 (1998-11-13) abstract	4
X	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 07, 31 July 1997 (1997-07-31) -& JP 09 081089 A (FUJITSU LTD), 28 March 1997 (1997-03-28) abstract	1
P,X	-& US 6 040 814 A (YOSHIOKA KOJI ET AL) 21 March 2000 (2000-03-21) see abstract column 1, line 49 - line 62 column 2, line 5 - line 25 column 5, line 32 -column 6, line 58; figures 3,4 column 8, line 15 - line 45; figure 8 column 9, line 4 - line 67; figure 9 column 10, line 63 -column 11, line 14; figure 13	1
A	US 5 250 937 A (KIKUO ONO ET AL) 5 October 1993 (1993-10-05) see abstract column 1, line 8 - line 60 column 2, line 3 - line 34 column 5, line 4 -column 7, line 37; figures 1,2,10 column 8, line 55 -column 9, line 10; figure 6 column 9, line 51 -column 12, line 43; figures 7-9 column 13, line 37 - line 68 column 16, line 26 - line 30; figure 11	1-5
X	US 4 714 921 A (KANNO HIDEO ET AL) 22 December 1987 (1987-12-22) see abstract column 1, line 8 -column 2, line 40; figures 3-6 column 2, line 65 -column 3, line 5 column 3, line 41 - line 61 column 4, line 19 -column 5, line 24; figures 1,2	1

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 00/09674

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		DE 3689153 D	18-11-1993
		DE 3689153 T	24-02-1994
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